**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICATION NO.: 10/606,462 EXAMINER: Sugent, James F.

FILED: 06/26/2003 ART UNIT: 2116

INVENTOR: Scott L. Michaelis *et al.* CONFIRMATION NO.: 3496

ATTORNEY DOCKET NUMBER 200205355-1

# REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Examiner's Answer, mailed 01/18/2008 in the above-captioned application.

A. Arguments regarding the First Ground of Rejection (claims 15-20 and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 7,103,639 (Walton)).

Claim 15

In applicant's appeal brief, applicant argued that claim 15 specifies reset code being executed by a processor in an existing partition, whereas Walton describes resetting of processors during partition formation. In the Examiner's Answer, page 10, the examiner cites Walton, column 3, lines 5-12. Note that Walton, column 3, lines 10-11 state: ". . . implements instructions executed on CPUs 302 pertaining to the partition formation process ..." (emphasis added). Accordingly, the examiner's own citation supports

applicant's argument that Walton describes partition formation, not resetting of an existing partition as specified in claim 15.

Claim 15 also specifies random access memory that is not affected by the reset code, that stores a list of addresses associated with the partition. In the Examiner's Answer, page 11, the examiner cites Walton, column 5, lines 23-31, referring to a "complex profile". In Walton, column 4, line 67 to column 5, line 22, the complex profile may include a data field associating cell 0 with partition 0, etc., but there is no discussion of addresses, and no discussion of the complex profile being in random access memory that is not affected by the reset code. The examiner states that the complex profile "inherently necessitates a list associated with the cell", and then states that such an inherent list must anticipate random access memory not affected by the reset code. Applicant respectfully submits that by the examiner's own characterization of a list, there is no necessity for such a list to include addresses, as opposed to mere associations as described in Walton at column 5, lines 13-15. In addition, a list of associations does not require random access memory that is not affected by the reset code (again, Walton is only describing partition formation).

Claim 20

Claim 20, dependent on claim 17, further specifies that each cell further comprises resources other than the at least one processor, and a portion of the resources is reset when the cell is reset. In the Examiner's Answer, pages 11-12, the examiner cites Walton, column 2, line 50 through column 3, line 22 for describing cells having resources other than the at least one processor, but neither the cited text or the examiner addresses resetting a portion of those resources.

Claim 23

Claim 23 specifies a list of reset register addresses, placing processors into a known state, and resetting by writing a reset code into the reset registers. In the Examiner's Answer,

page 12, the examiner argues that the complex profile discussed in conjunction with claim 15 inherently necessitates storing addresses of reset registers. Again, as discussed by applicant in conjunction with claim 15, there is no necessity for such a list to include addresses, as opposed to mere associations as described in Walton at column 5, lines 13-15.

In addition, the examiner states without citation that writing a reset code into reset registers is inherently necessitated to reset a PC family. That inherency argument conflicts with the present application. In the present application, reset registers are an attribute of cells, not processors (paragraph [0022]). Partitions comprise cells (figure 2), cells comprise processors and cell controllers (figure 3), and the cell reset is initiated by writing a reset value to a register in the cell controller (paragraph [0016] and paragraph [0023]). The cell controller then resets processors by sending an interrupt to the processors, which causes the processors to read the value in the associated status register in the cell controller (paragraph [0023]). Therefore, the reset registers are not inherent to a PC family.

B. S

econd Ground of Rejection (claims 1-13 are rejected under 35 U.S.C. § 103(a) over Walton in view of U.S. application publication number 20030236972 (Harrington)).

Claims 1-3, 5-7, 9-10, and 12

Claim 1 specifies sending an interrupt to the other processors. In the Examiner's Answer (page 6), the examiner submits that Walton, figure 2, steps 206 or 208, show sending an interrupt. Step 206 merely says "reset cell" and step 208 merely says "synchronize cells", with no teaching or suggestion that those steps include interrupts. In the Examiner's Answer (page 13), for this limitation, the examiner rests on arguments made in association with claims 15 and 23. However, neither claim 15 nor claim 23 includes sending an interrupt to the other processors, and no argument was made for that

limitation in conjunction with claims 15 and 23. Accordingly, no *prima facie* case for obviousness has been established.

Respectfully submitted,
KLAAS, LAW, O'MEARA & MALKIN, P.C.

By: /Augustus W. Winfield/

Augustus W. Winfield, Reg. No. 34046
1999 Broadway, Suite 2225
Denver, Colorado 80202
Telephone: (303) 298-9888

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